REMARKS / ARGUMENTS

Claims 21, 23-25, 27, 29-39 and 44-54 remain pending in this application. Claims 22, 26 and 28 have been canceled without prejudice or disclaimer. No new claims have been added.

Interview

Applicants wish to thank the Examiner for conducting an interview with the undersigned and Applicants' representative on August 25, 2008. The following includes the substance of that which was discussed during the interview.

Claim Objections

The claims have been amended to overcome the Examiner's objections. No new matter has been added.

35 U.S.C. § 103

Claims 21-28 and 30-52 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hubis et al (U.S. Patent No. 6,343,324) in view of Katzman et al (U.S. Patent No. 4,228,496). Claim 29 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hubis et al, in view of Katzman et al and further in view of Kuchta at al (U.S. Patent No. 6,014,319). Claims 53 and 54 stand rejected under 35

U.S.C. §103(a) as being unpatentable over Hubis et al in view of Katzman and further in view of Matsunami et al (U.S. Pub. No. 2002/0091898). These rejections are traversed as follows.

As explained during the interview, according to the present invention, the number of processor adapters (units) of the storage system can be increased or decreased, independently of the first and second interface adapters (units), the memory adapter (unit) and the switch adapter (unit). None of the cited references disclose or suggest the claimed feature of the present invention.

As admitted by the Examiner, Hubis et al do not disclose a plurality of processor adapters, the number of which is increased or decreased based on a required performance. The Examiner relies upon Katzman for curing this deficiency. However, such combination fails to render the claimed invention unpatentable for at least the following reasons.

Katzman et al disclose a processor module having an inter-processor control 55, a CPU 105 and a memory 107, all of which are at a higher level than I/O channel 109. Therefore, the processor module is at a higher level than the storage system and may correspond to a host device, for example. On the other hand, device controller 41 of Katzman et al is coupled to disks 45 and can be said to correspond to the storage system of Katzman et al.

In Katzman et al, the number of processor adaptors would not be increased or decreased independently of another kind of adaptor (or unit) including the first and second interface adaptors, the memory adaptor and the switch adaptor as now

claimed by amendment. It is pointed out to the Examiner that claim 39 does not recite a switch adapter.

Furthermore, the memory adaptor presently claimed has a memory for temporarily storing data sent from the first interface adaptor(s) (unit(s)). On the other hand, Katzman does not disclose any such memory between I/O channel 109 and device controller 41. Therefore, Katzman does not have any memory adapter as presently claimed.

The deficiencies in Hubis et al and Katzman et al are not overcome by resort to any of the remaining references. As such, it is submitted that the pending claims patentably define the present invention over the cited art.

Conclusion

In view of the foregoing, Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.

By /Shrinath Malur/
Shrinath Malur
Reg. No. 34,663
(703) 684-1120